Three Thermal Simulation & Test Innovations for Electronics Equipment Design

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DENSO
Crafting the Core

Over the last 50 years the automotive industry has been going through huge shifts in electrification (Figure 1). And, of course, we are seeing the electric motor starting to replace the mechanical engine with the advent of Electric & Hybrid Vehicles. Not surprisingly, the demand for ever higher density in a confined electronics, leads to a greater and greater need to resolve the resultant thermal issues.

Thermal simulation technology for automotive electronic equipment design is shifting from steady state to transient analysis. Here, I explain detailed Data Network Resistance Capacitance (DNRC) transient models, which are based on Mentor's T3Ster® tester data. In this article, three innovations to methods for creating DNRC models useful in electronics thermal design are outlined:

1. Placement of measurement locations in models so that the gap between actual measurement and analysis can be identified

2. Preliminary verification of component Tj (junction temperature) value by CFD thermal analysis

3. Creation of compact models from manufacturer datasheets and Tj calculations – what we call a DSRC, Datasheet Resistance Capacitance model.

If we consider a typical automotive engine control unit (ECU) in Figure 2; it can be noted that a typical engine underhood compartment in a car hits relatively high temperatures of approx. 105°C and since electronic parts typically have an upper practical operating limit of which threshold must not be surpassed otherwise electronic component quality cannot be guaranteed.
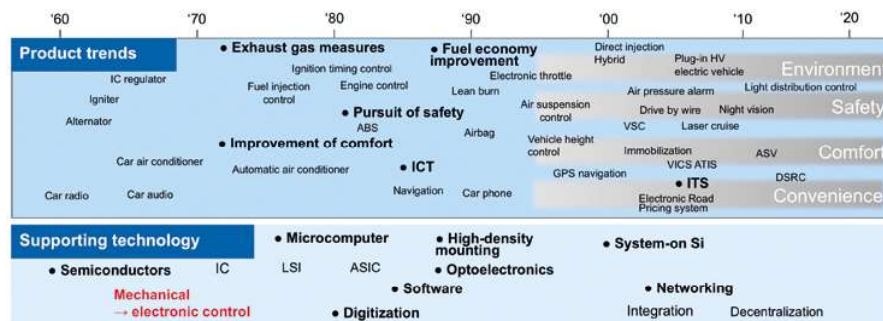

Figure 1. Progression of car electronics product adoption and underlying trend over the last 50 years
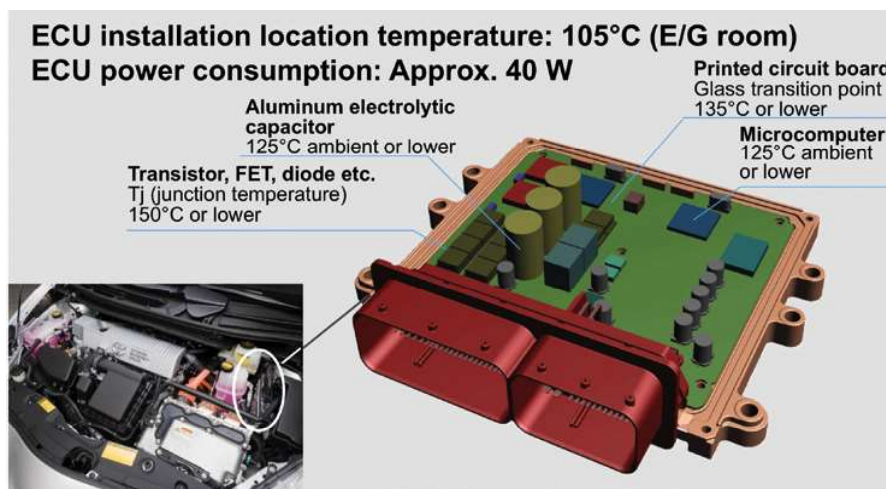

Figure 2. Typical ECU and engine use case and thermal limits

Moreover, we are seeing that with the advent of more vehicle electrification and with autonomous vehicles on the horizon (Figure 3), there is a need to thermally simulate transient heating effects in ECUs more and more, especially while the advent of Advanced Driver-Assistance Systems (ADAS) increases the number of high-frequency ECUs. Hence, it is necessary today to be able to estimate instantaneous heat generation inside ECUs. Transient thermal analysis needs by JEITA in 2013 were identified to be:

- Tj response during LED lighting operation,

- Instant transient analysis of Transistor, FET, IC and other semiconductors; with measurement of junction temperatures,

- Hot spots during SoC (System on Chip) operation,

- Tj response from engine OFF (dead soak), and

- Business need for the verification of accuracy between measurements and thermal analysis.

The target times for transient thermal analyses depends on whether we are dealing with a chip, a package or an assembly (like an ECU) as illustrated by Figure 4.

From the early days of the electronics cooling simulation market there has been some sort of approximation of chips and packages in terms of their thermal performance and the details inside the chip. DELPHI compact thermal models appeared in the 1990s and quickly became the standard way of modeling packages for CFD simulation that also allows for manufacturers to protect their intellectual property. However, the models do only satisfy transient analysis in terms of the accuracy, because the DELPHI compact thermal models are solely represented by thermal resistance values. Figure 5 depicts Denso's way of looking at all types of analysis models that could be employed to solve our thermal simulations. It is the DNRC and DSRC models that we want to investigate in this study because of their inherent high accuracy and ability to be distributed into the semiconductor supply chain. Based on non-destructive electronics thermal transient testing methodology, DNRC is modeled by 'structure functions, featured by Mentor T3Ster tester (Reference 1). While the form of DSRC is the same as that of DNRC, DSRC model is based on the transient response values in IC component datasheet.
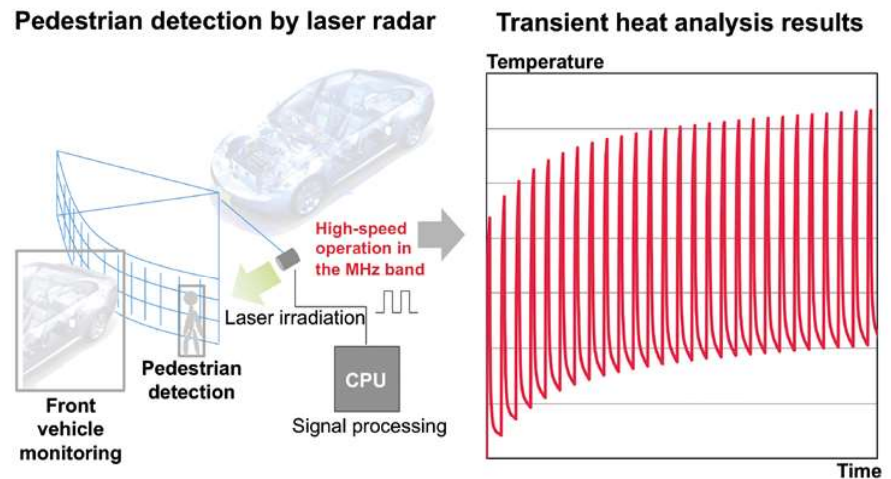

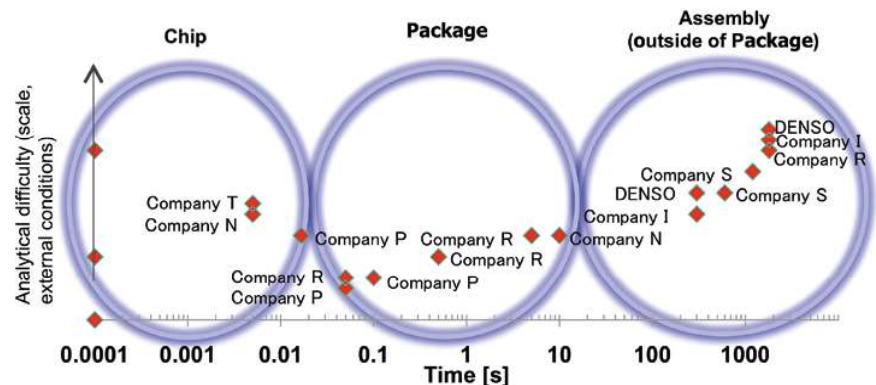Figure 3. Escalation of transient heat issues with ADAS technology

Figure 4. Target time for transient thermal analysis for Chips to Assemblies
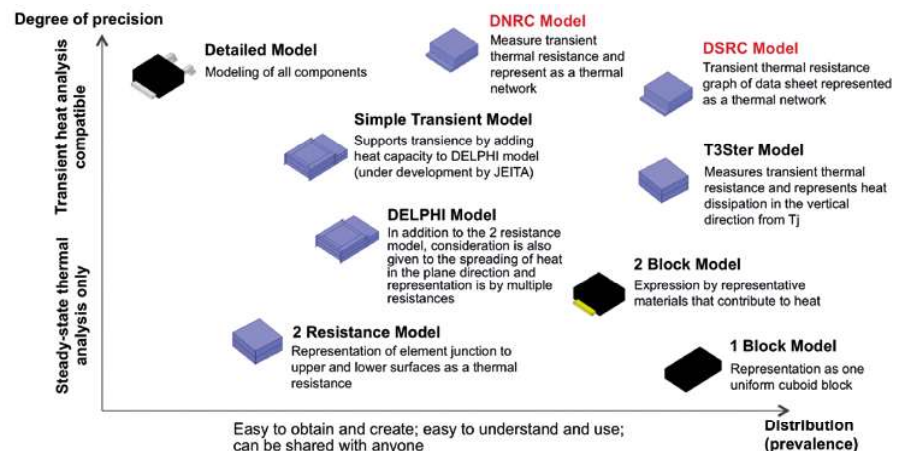

Figure 5. Development of package element models that meet ECU transient thermal analysis needs

This article is not going to go into the details of the T3Ster RC approach for measuring electronic element constituent performance, and how it connects to CFD simulation thermal analysis tools like FloTHERM – see Reference 2 for further details. However, an outline thermal simulation & test workflow is shown in Figure 6 that results in a useful
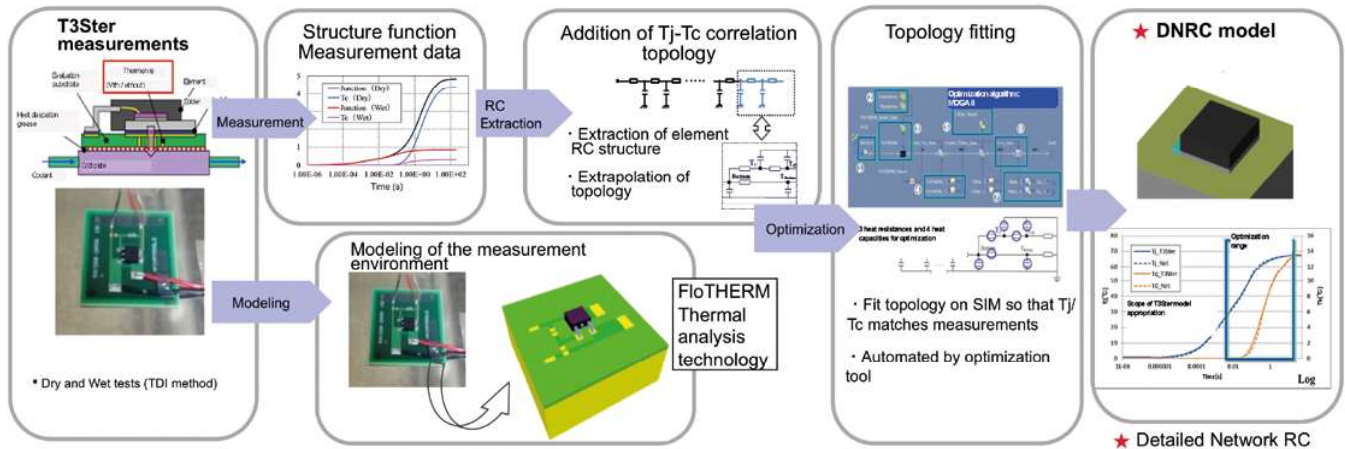
Figure 6. Outline of RC model creation process for a DNRC model by T3Ster measurements & FloTHERM simulations

DNRC model. Here, I emphasize two advantages as below.

- The approach allows for reference point thermal measurement of components in their mounted state on a PCB
- The measured data can be fed into CFD simulation software such as FloTHERM™

Indeed, the beauty of this approach is that it is possible to create a model even if information such as internal dimensions, specific heat, performance etc. of the component is not readily available. The final DNRC is very high precision, because the model is derived by measuring the thermal resistance and thermal capacitance values. Moreover, because DNRC is a thermal network model and has the Tc node existing for verification by measurement with a thermocouple, the values of the model can be compared with the actual temperature measured at Tc for reconciliation. Crucially, this modeling approach can be used by a component manufacturer who does not know the internals of the elements involved. We have completed a validation study (Figure 7) for a typical electronics component package and heatsink array which calculated the relative accuracy of the different types of models outlined in Figure 5. Using the 'Sum of Squares' error estimation method it can be seen that the most accurate approach (the lowest number in the table) is the DNRC approach.

If we now apply this approach to the measurement of transient thermal resistance of a PCB, it is then desirable to measure both the semiconductor component and the PCB simultaneously. We did this with an experiment involving two test circuits with different thermal resistance and
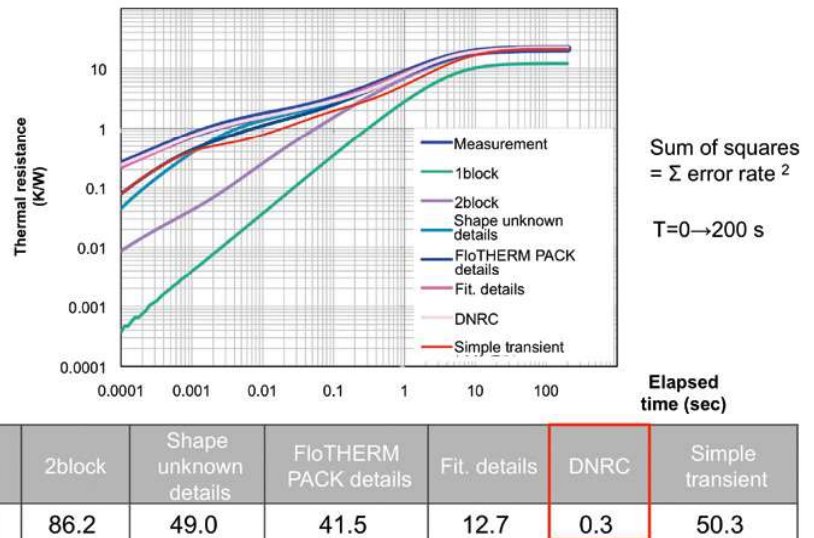

Sum of squares
= Σ error rate ^{2}

T=0→200 s

1block	2block	Shape unknown details	FloTHERM PACK details	Fit. details	DNRC	Simple transient
121.0	86.2	49.0	41.5	12.7	0.3	50.3

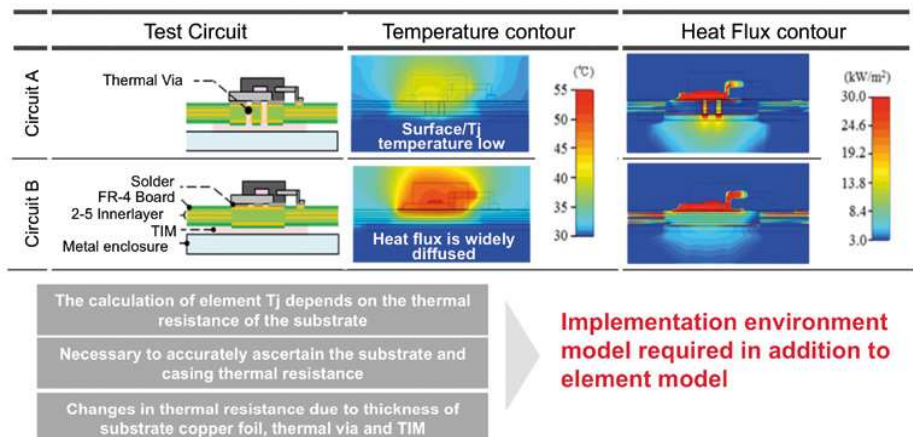**Figure 7.** Results of element model accuracy verification Predictions versus Measurements

Figure 8. FloTHERM simulation verification of element temperature and heat flux distribution for a circuit with and without a thermal via

capacitance values – one with a through silicon via and one without (Figure 8). The choice of the through Si via meant that the thermal resistance of the PCB without it is overwhelmingly higher than that of the element as a whole – the element being 3K/W with the substrate at 10-20 K/W. Hence, these simulations prove that an environment model in which the element model is located matters and is required for accurate results. There needs to be measurements with T3Ster of the transient thermal resistance of the element in mounted state on the PCB so as to produce thermal resistances equivalent to those in the actual product. This can be seen in Figure 9 where T3Ster confirms the thermal resistance at each point of the two circuits with and without vias being considered in the study. We even examined slight knicks (cracks) in the two structures and saw that structure functions of inside and outside the semiconductor could be discerned correctly.

If we use T3Ster measurement result to calibrate a detailed thermal model for FloTHERM, we devised a seven step workflow process (Figure 10) to accurately obtain the physical property values of any PCB. It involves using FloTHERM coupled with powerful design space optimization tools in order to search for the optimal solution to curve fit onto the actual T3Ster measurements. This in turn reveals accurate physical property values in terms of the thermal conductivity and specific heat of the actual substrate layers. This data can then be used as shown in Figure 11 to evaluate the two circuits we described earlier. And we were able to simulate 1,000 designs in FloTHERM and fit the results to the structure functions under actual measurement. However, the thermal conductivity in copper foil shows 485W/mk, which is not a realistic value, assuming the thermal conductivity for pure copper is as low as 398w/mk. Finally, we were able to do microscopic cross-section measurements (Figure 12) of the PCB substrate with different layers of copper foil thicknesses as a cross-validation of this T3Ster and FloTHERM approach. It revealed that the copper foil is 1.3 times thicker than the design data. When it is converted to the thermal conductivity, it becomes 1.3 times. We got remarkably good agreement and it shows our approach is valid.

The biggest issue facing manufacturers and assembly makers is in measuring actual Tj values (Figure 13). Device manufacturers usually guarantee their electronic components to less than 150°C but how
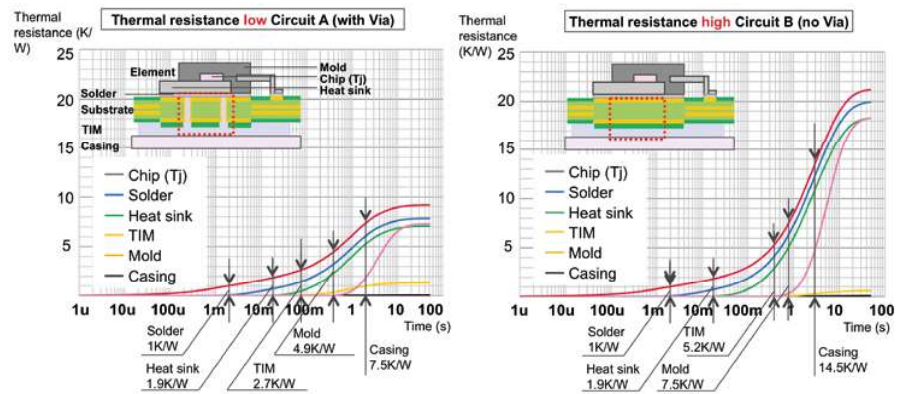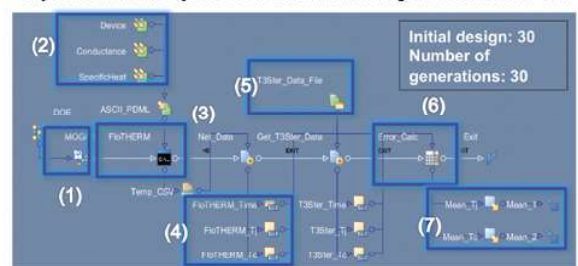

Figure 9. Temperature rise start time and thermal resistance of component for a circuit with and without a thermal via using T3Ster

Figure 10. Method of determining physical property values of printed circuit boards (PCBs) using FloTHERM and T3Ster
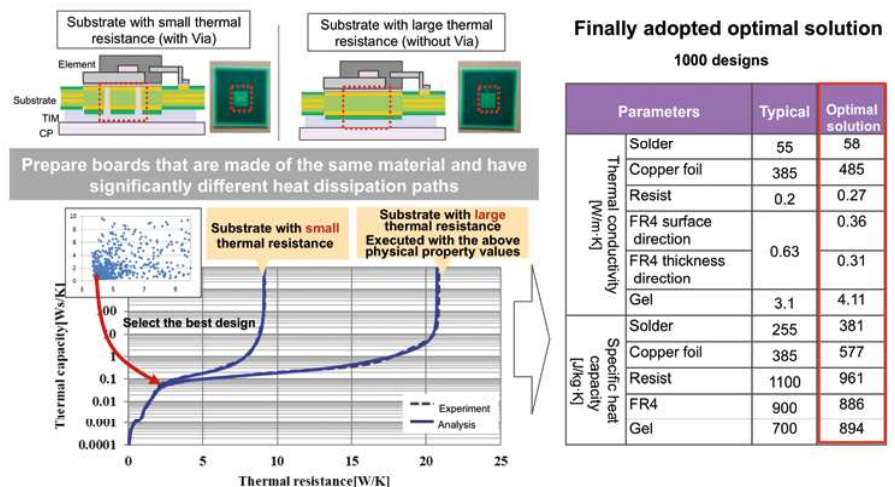

Figure 11. Optimal circuit thermal solution selected from multiple designs

to measure Tj accurately and how to see instantaneous changes in temperature as the device operates? Usually the Tj can be measured by a thermocouple and derived from an electric power waveform analysis and transient thermal graph in datasheet (Figure 13).

If we look at our first proposed innovation, that is, the temperature of the part for coupling with thermal analysis is known. Figure 14 shows this for Tc and Tj values with the various model types outlined in Figure 5. With detailed model and DNRC model, the Tc node enables a comparison with experimental results to ascertain the error of the CFD thermal analysis.

Our second innovation, preliminary verification of the Tj value by FloTHERM thermal analysis is shown in Figure 15. It can be seen that only a detailed DNRC model with a Tc node derived from FloTHERM and T3Ster works well and internal package information is simulated accurately such that a transient Tj and Tc can be estimated in a short period of time.

Our third innovation is that it is now possible to create models based on manufacturer's datasheets and calculate actual Tj values. This is shown in Figure 16 where it can be seen that a DNRC model captures the actual transient thermal resistance in the component's mounted state thus leading to an ultra-high precision model that conforms to actual operating conditions. On the other hand, a DSRC model is based on a transient thermal resistance graph. Hence, the value in the datasheet and the DSRC model based on the datasheet are both guaranteed by the manufacturer. Table 1 shows a relative comparison between the recommended usage of DRNC and DSRC models. As noted in the table, a DSRC approach is a great bridge between analysis models and component manufacturer's guaranteed property values in their datasheet. Moreover, as the DSRC matches the manufacturer's datasheet value, it can be guaranteed for product design. If the data applicable in product design can be converted into a model for analysis, both component manufacturer and assembly maker can easily exchange the models, hence both welcome the approach. Another benefit to this approach is relatively lower costs compared with other measurement techniques that have high measurement and labor costs.

Finally, we carried out a validation test in a standard transient thermal analysis JEDEC still air chamber of a component on a PCB

Substrate configuration

6 layer penetration (newFR4 t1.2)
40*40 Inner layer residual copper ratio 80% solid
Wiring: 4 terminal method
Wiring: Short circuit possible between D - G and G - S
Outer layer pattern 18 + 25 μm
Inner layer pattern 35 μm
AW shape on the reverse is □ 10 in center of the thermal via

Substrate layout
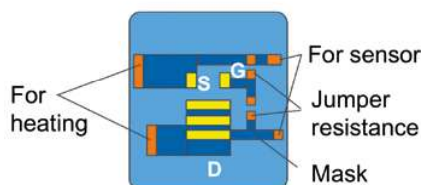
Optimal solution

Material	Thermal conductivity [W/m·K]		Specific heat capacity [J/kg·K]	
	General value	Optimal solution	General value	Optimal solution
Solder	55	58	255	381
Copper foil	361	485	385	577
Resist	Approx. x 1.3		Approx. x 1.5	
FR4	0.63	0.36	900	886
Gel	3.1	4.11	700	894

Microscope cross section measurement

52.4 μm
50.0 μm
42.8 μm
42.8 μm
45.2 μm

1.3 to 1.4 times the 35 μm of copper foil, which generally agrees with the magnification from the reference value of the optimal solution.
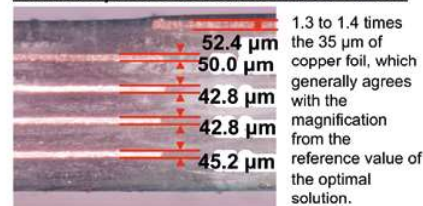
Figure 12. Validation of optimal solution with a structural survey of real substrate samples
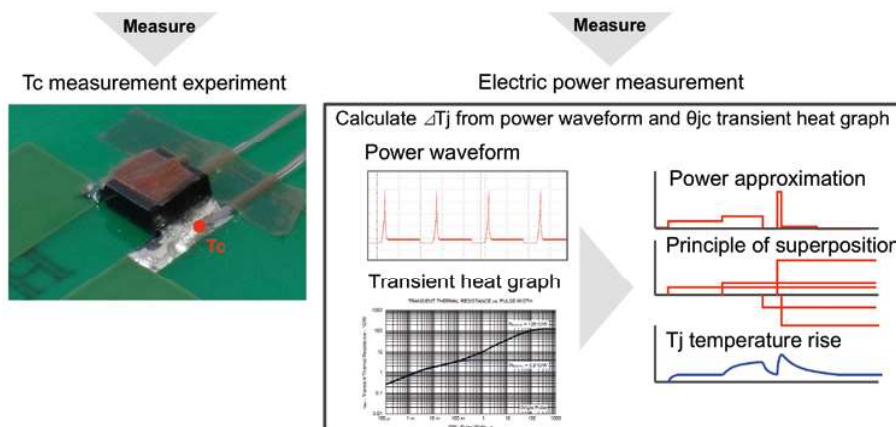

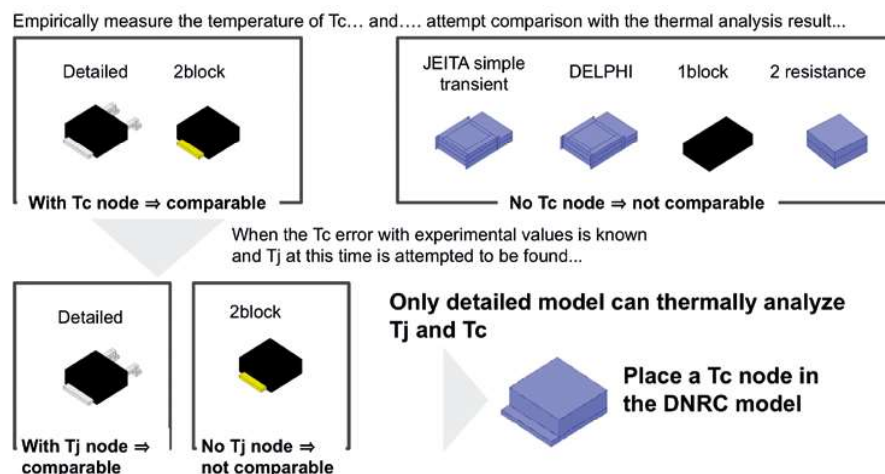**Figure 13.** Issues in finding Tj by thermal design for a circuit

Figure 14. Innovation 1 - Temperature of the part for coupling with CFD analysis is known

	DNRC model	DSRC model
Design phase of model use	Verification of prototype	Concept only
Product status	Actual product assembly	Evaluation environment defined b standards
Transient thermal resistance	Measurement	Manufacturer's guaranteed datasheet value

This is important

**Table 1.** Comparison of DNRC models and DSRC models for thermal analysis

(see Figure 17) and compared it with the T3Ster and FloTHERM approach outlined above. Error rates were very low and good agreement in the DSRC models to the manufacturer's datasheet values were observed. Hence, DSRC model creation based on manufacturer's datasheet is possible and improved accuracy can be achieved by these in-built substrate models.

Summary

We have shown that by using a coupling of Mentor's T3Ster transient thermal testing hardware and FloTHERM thermal analysis CFD software it is possible to measure thermal resistance of PCBs accurately and to create thermal simulation models of semiconductor component by using DNRC models for unsteady state analysis. The DNRC modeling approach outlined here allows for the calculation of Tj values with a high level of accuracy in the CFD analysis technology. Comparative verification with measurements by Tc nodes are shown to be possible such that the approach is useful for verification experiments. Furthermore, DSRC based on datasheet value can be used for thermal design according to the manufacturer's datasheet values.

References

[1] Rencz, M. & Székely, V.,"Measuring partial thermal resistances in a heatflow path". IEEE TRANSACTIONS ON COMPONENTS AND PACKAGING. 25 (4): 547–553, 2002.

[2] Bornoff, R. & Vass-Varnai, A., "A detailed IC package numerical model calibration methodology", 29th SEMI-THERM Conference, pp.65-70, 2013.
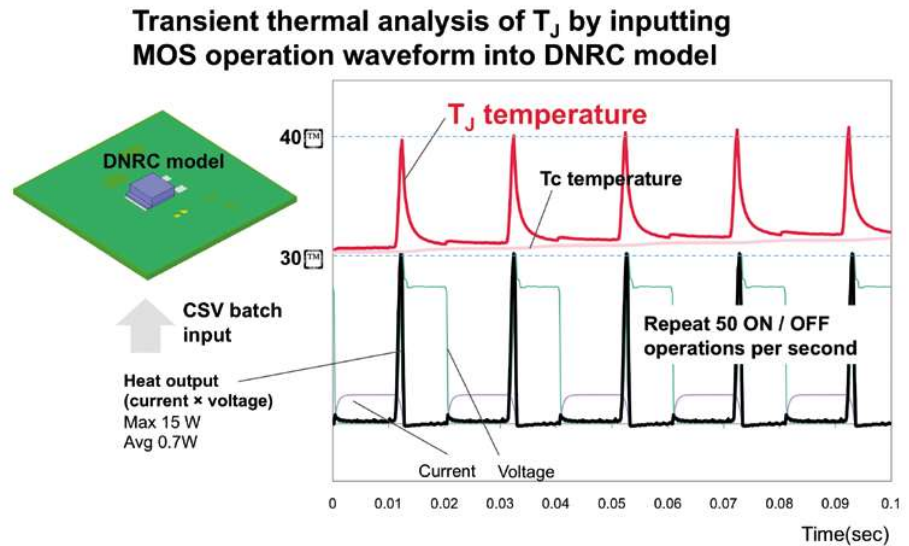
Figure 15. Innovation 2 - Preliminary verification of Tj value possible by FloTHERM thermal analysis
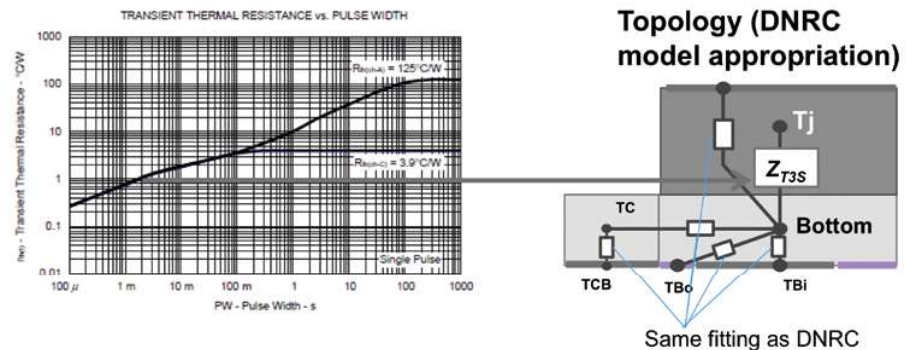
Figure 16. Innovation 3 - Possible creation of models from manufacturer datasheets and calculate Tj
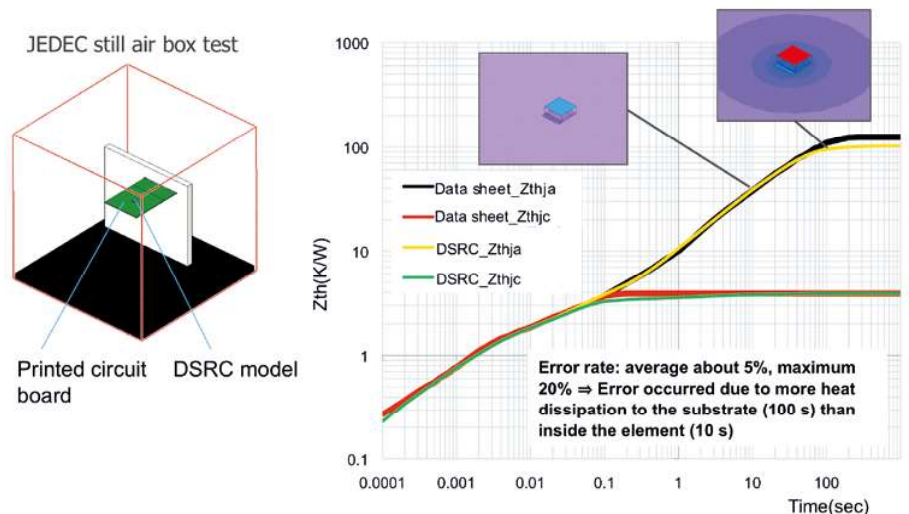
Figure 17. Experimental Validation - Transient thermal analysis in JEDEC environment according to the measurement environment of a component's datasheet value