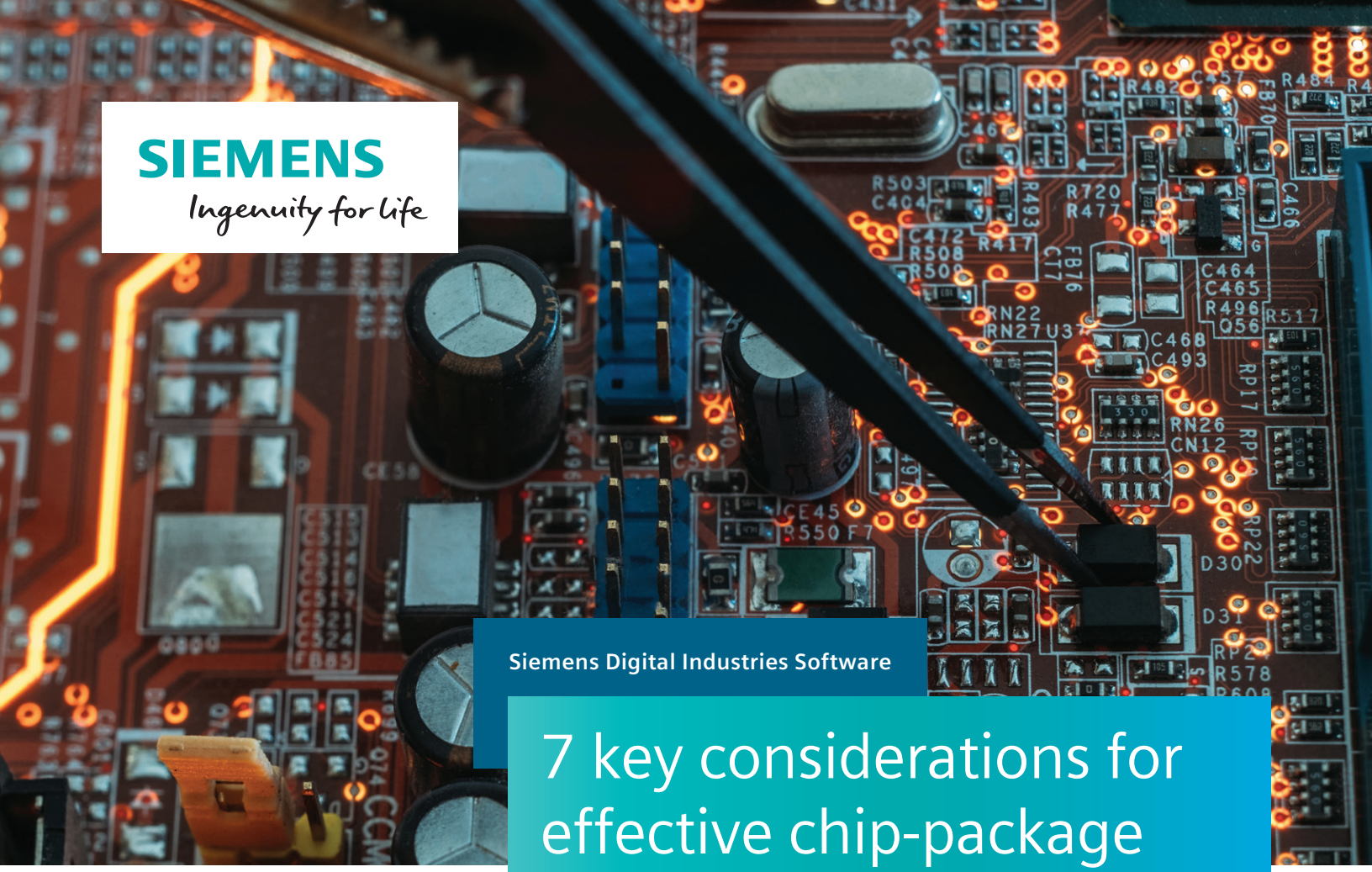

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7 key considerations for effective chip-package thermal co-design

A high-level 'how to' guide

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Why is chip-package thermal co-design important?

Chip-package co-design is important for several reasons. Designing a large high power die, e.g. a System-on-Chip (SoC) without considering how to get the heat out is likely to lead to problems later on, resulting in a sub-optimal packaging solution from cost, size, weight and performance perspectives. Historically IC design has considered the die temperature to be uniform. This is no longer a valid assumption in many cases. Heating due to current leakage, which is temperature dependent, is making power dissipation less uniform, and the use of thinner die, now well below 50µm, has reduced the heat spreading capability of the die itself. Both of these effects contribute to greater on-die temperature variation.

When is chip-package thermal co-design essential?

Chip-package co-design becomes essential when designing stacked Three-Dimensional Integrated Circuits (3DICs). The dies cannot be designed independently due to their electrical and thermal interaction. Through Silicon Vias (TSVs) that act as inter-die interconnections can help get heat out of the die stack, although their primary role is in reducing hot spots, so their placement relative to high power regions on the die can have a marked effect on the overall thermal performance. Conductive heat transfer is a highly 3D phenomenon so the package temperature distribution affects the temperature distribution on the die.

1. Always start with the package

To get the correct temperature distribution within the die, it's essential to include the package construction in the thermal model, mounted on a typical PCB and where appropriate with a representation of a heatsink solution, so that the effect of heat spreading in the board and into the heatsink are accounted for in the predicted package temperature distribution. For this a full computational fluid dynamics (CFD) simulation is required to correctly predict the way the package interacts thermally with its environment, and hence predict the correct temperature distribution within the package itself.

Note that simply applying a constant thermal resistance value to each surface of the die to represent the heat flow path to the ambient is not sufficient as a boundary condition. A high resistance to the ambient does not capture any local heat spreading effects due to the presence of high thermal conductivity materials in close thermal contact with the die itself. These tend to hold the die temperature uniform without contributing significantly to the total thermal resistance to the ambient. Using a single thermal resistance value may lead to over, and possibly incorrect design decisions.

In early design, and before the detailed IC design starts, there is the greatest scope for optimizing the chip-package architecture. At this stage the number of die, and the intended size and budgeted power for each die will be known. This can be used to create a 3D thermal conduction model (which could also include convection and radiation if the package style includes an internal cavity) of the candidate package(s) that can be used to explore the package design space. This model also provides the thermal environment that will allow temperature data to be back-annotated to the IC design flow.

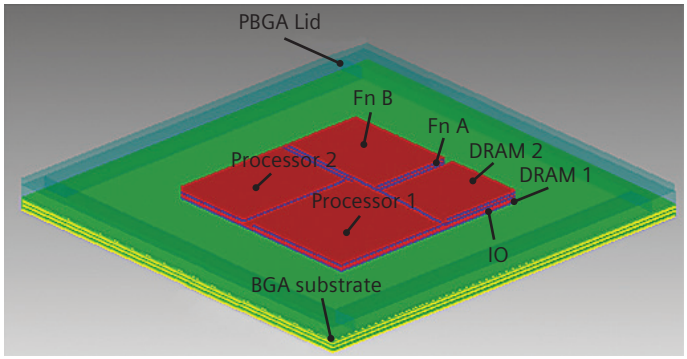

Figure 1: Detailed thermal model of a BGA package with multiple die.

2. Explore the package design space before the IC design starts

The thermal model of the candidate package(s) can be used to investigate the influence on the thermal performance of different die arrangements, package size and packaging materials, for example the amount of copper in the substrate for a Ball Grid Array (BGA) package.

At this stage there is a high degree of freedom, and hence opportunity, to explore different package options, and the design of each. Based on an initial estimate for the size of the die, design parameters that can be investigated to determine their influence on the die temperature rise and variation for a given package style may include:

- Influence of the number and possible layout of TSVs
- Influence of the size, shape, and material choices for an interposer
- Effect of interfacial resistances (glue layers)
- Pyramid vs. overhang stack arrangements (if wire bonded)
- Cooling solutions internal to the package, e.g. die edge cooling, internal heat slugs, etc.
- Influence of external cooling solutions, e.g. solder pads, underfill options etc.

Features that have the greatest effect on die temperature rise and variation self-indicate the need to be modelled in greater detail, and optimized for thermal performance.

3. Include temperature dependent thermal properties

This is automatic for silicon and other materials included in Simcenter Flotherm's material library. Temperature ranges across the die are likely to be too high to assume a single thermal conductivity value, so temperature-dependent thermal conductivities are necessary to accurately predicting die hot spot values. Note that for transient calculations it is essential to include the material density and specific heat capacity. This happens automatically in Simcenter Flotherm™ software when a material is attached to an object.

4. Refine the die surface treatment

Include a 3D representation of the active layers of the die (metallization and polysilicon) with an isotropic block ~0.5 to 1.0 µm thick.

Silicon dioxide (SiO2) and silicate glass, typically used as dielectric materials to separate metal wires on the active surface of the die have thermal conductivities of the order of 1 W/mK, around two orders of magnitude less than the metal they isolate, historically being aluminium or copper. Wires on different levels run in different directions, so the material behaviour is locally orthotropic. However, the high level of interconnection between the levels, combined with metal running in different directions, causes the heat to smear. Hence for early design activities outside the main IC design flow the bulk behaviour can be approximated with an isotropic material with all the active surface layers captured within the thickness of one mesh cell in the package-level model.

The IC process and design technology files contain information about metal width and spacing as well as the preferential routing directions. This can be used to calculate the overall thickness and an isotropic averaged material property for this thermally-active layer.

5. Back-annotate temperature information before floorplanning

Up to this stage heat should be distributed uniformly over the die. This will not be the case in practice, and the model should be refined to remove this assumption as soon as more detailed information is available from the IC design team. The benefit of using this assumption at the outset is that it gives an indication of the inter-die temperature variation that arises from the package's limited ability to hold the bulk die temperature uniform.

Providing the IC design team with information about the average die temperature and temperature variation for each die before the IC design process starts can greatly help floorplanning [ref. 1], which is critical to the quality of the design, as decisions made during floorplanning can either alleviate or exacerbate this temperature variation.

6. Use power budgets during floorplanning

Once floorplanning starts, get a high-level power map from the IC design team and import that into the thermal model of the package. Simcenter Flotherm has a Die SmartPart that allows powers to be read in as a CSV file so this can be done automatically and the results quickly fed back as the simulation model will often only take a matter of minutes to run, indicating where TSVs can be introduced to improve the thermal performance, or where design changes are needed. For example, it may be important to ensure that two or more different functional blocks operate at very similar temperatures to eliminate timing issues.

For logic-on-logic 3DICs this should be accounted for when partitioning the design amongst the various dies, and during inter-die and intra-die floorplanning, requiring power map information for each die. At this stage opportunities exist to move the functional blocks in both x- and y-directions (xy expansion) keeping their relative positions the same but adjusting the gaps (white space) between them into which TSVs can be inserted to examine their impact on die hot spots. Knowing the TSV size and pitch, which scale with die thickness, blocks of higher through-plane thermal conductivity can be superimposed over the die thickness in these white space regions in Simcenter Flotherm, to locally override the properties of silicon.

In early floorplanning extremes can be investigated to inform the IC design team of the extent to which hot spots can be controlled using TSVs, bounding the problem. Optimizing both functional block and TSV layouts during floorplanning needs to be done as part of the IC design flow.

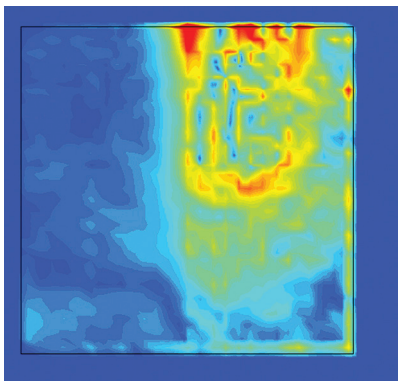

Figure 2: Die temperature distribution due to detailed non-uniform power map

7. Closing remarks: Make the IC design flow temperature aware

As floorplanning progresses, the thermal design effort needs to focus on the detail of the thermal interaction between die as the design is further elaborated. The power map for the die becomes much more detailed, and in the case of a 3DIC, the number and location of TSVs need to be defined as part of the electrical design.

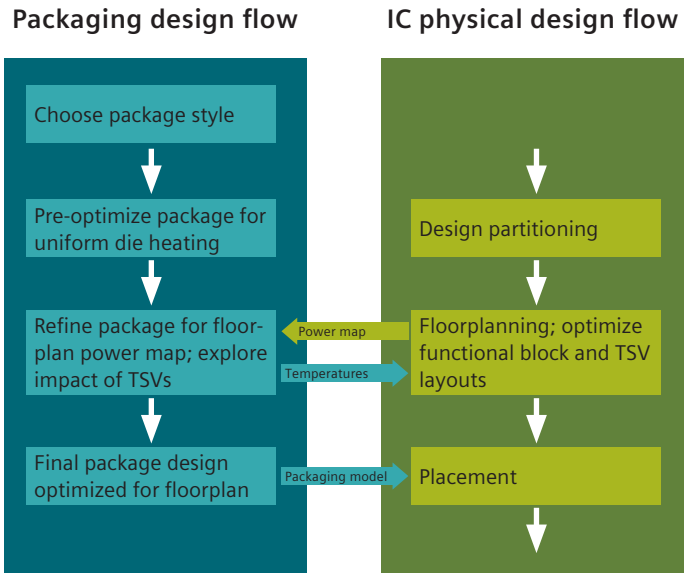

Figure 3: Opportunity for parallel package and IC physical design flows [ref. 2]

This work is best done within the IC design flow itself, and to this end Simcenter Flotherm has been embedded into Simcenter's Calibre suite. Simcenter has partnered with TSMC to create a thermal analysis flow based on Simcenter Flotherm and Calibre DESIGNrev and RVE, an industrial standard physical verification results viewing environment [ref. 3]. It provides an easy-to-use, fast and accurate tool to do thermal simulation on dies and interposers of 3DIC, enabled by automatic gridding built into this solution that uses a localized grid in critical model areas such as the dies.

3DIC reference flow – Simcenter track

Physical implementation • Cross-die bump mapping • TSV/ubump and back-side metal routing • Cu-pillar bump implementation	**Olympus-SOC**
Custom design • Support die-stack configure file and bump file • Schematic-driven design support TSV feed-thru	**Pyxis**
DFT • Pre-bonding – Die level testing (logic, memory) • Pre-bonding – IO wrap test • Post-bonding – Interconnect testing • Post-bonding – Pattern retargeting (die to stack)	**Tessent**
Reliability • Static/transient die-stack thermal simulation	**Calibre 3DSTACK/Simcenter Flotherm** **Calibre DESIGNrev/Calibre RVE**
Physical verification • Inter-die DRC/LVS support • LVS for double-side bumps (DEF/GDS)	**Calibre 3DSTACK** **Calibre nmRDC** **Calibre nmLVS**
RC extraction • RCX for double-side bumps (DEF/GDS) • TSV-to-TSV coupling RCX for STA/spice • TSV subckt replacement for RLC-model	**Calibre xRC**
SPICE timing analysis • Multi-technology SPICE simulation	**Eldo**

Figure 4: TSMC 3DIC reference flow 2013 [ref. 3]

This solution takes die power map files that can be generated by power analysis tools, and creates thermal maps that can be used for thermal design and for checking against thermal constraints. The thermal results can also be displayed as a histogram in Calibre RVE, and the thermal hotspots highlighted onto the design in Calibre DESIGNrev. In transient analysis, temperature vs. time graphs can be displayed using Simcenter EZwave, a high-capacity, high-performance graphical waveform environment.

More accurate thermal models of dies that take into account the metallization, such as interconnects and TSV in the dies, can be created and used in thermal simulation. A 3DIC thermal model can be created to allow the 3DIC package to be imported into a larger system, for further thermal simulation at the system level.

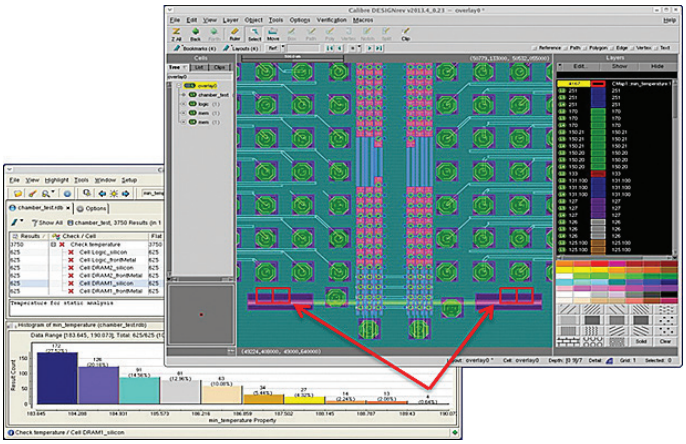

Figure 6: Thermal histogram in Calibre RVE and hostpot overlay in Calibre DESIGNrev

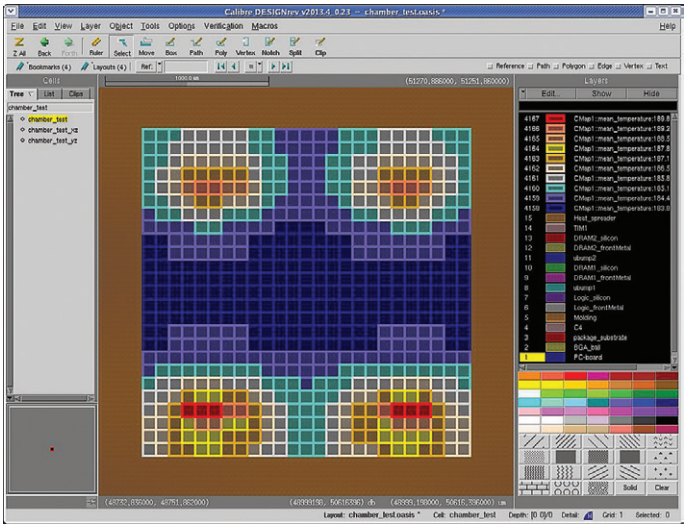

Figure 5: Thermal colormap in Calibre DESIGNrev

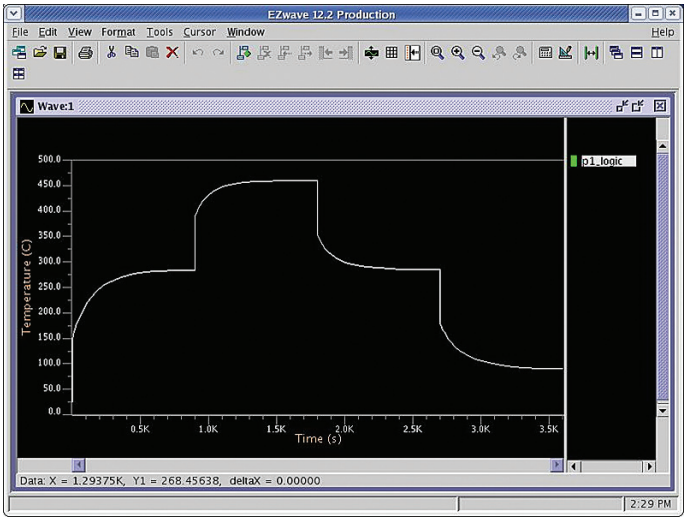

Figure 7: Temperature versus time curve displayed using Simcenter EZwave

Acknowledgements

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